

In item 4 on page 3 of the above-identified Office action, claims 9 and 12 have been rejected as being indefinite under 35 U.S.C. § 112, second paragraph.

More specifically, the Examiner has stated that a link region between the base region and a polysilicon track and the formation of an emitter are not shown or described.

With respect to claim 9, according to page 10, lines 12-16 of the specification, the second region refers to the area provided with a higher dopant concentration (see also preamble of claim 1: "... such that a first region of the two adjacent regions has a target concentration of a dopant that is lower than a target concentration of the dopant in a second region of the two adjacent regions."). In addition, please compare page 20, lines 24-26 ("A lower dopant concentration 12d results in the actual active area of the base, and a higher dopant concentration 12c results in the link area underneath the spacer 9.") and page 5, lines 14-18 ("In addition to the emitter window, further structures of the semiconductor are illustrated, namely two isolation layers 2 and 3 and a polysilicon layer 4 that constitutes the polysilicon track that is formed as an external component of the base of the transistor to be formed.") of the specification. In summary,

the second region 12c represents a link region between a base region 12d and a polysilicon track 4.

With respect to claim 12, as mentioned in the previous paragraph, the first region refers to region 12d. Therefore, according to page 12, line 8 of the specification ("*...and the first region forms a base area under the emitter.*"), the emitter is above region 12d, surrounded by the spacers 9 (see page 12, line 7) within the so called emitter window 1 (see page 5, lines 11-13: "*The emitter window 1, which is placed in the area of the subsequent active transistor...*").

Therefore, a link region between the base region and a polysilicon track and the formation of an emitter are clearly shown in the drawings and described in the specification.

It is accordingly believed that the claims meet the requirements of 35 U.S.C. § 112, second paragraph. Should the Examiner find any further objectionable items, counsel would appreciate a telephone call during which the matter may be resolved.

In item 2 on page 2 of the above-mentioned Office action, claims 1-12 have been rejected as being unpatentable over disclosed prior art and further in view of Glang et al. (US Pat. No. 4,467,519) under 35 U.S.C. § 103(a).

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and the claims have, therefore, not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

diffusing the dopant outward from the first region until the concentration of the dopant corresponds to the target concentration of the first region.

The Examiner has referred to the text in column 6, lines 41-50 of Glang et al., which reads:

"A second annealing step is utilized to fully drive in the boron to form the base region and simultaneously therewith drive in the arsenic to form the emitter region of the transistor. This process involving a two-step annealing process for the boron implanting ions is necessary to create a base with sufficient width and doping to avoid punch-through."

as disclosing the step:

"diffusing the dopant outward from the first region",
as recited in claim 1 of the instant application.

Applicant respectfully disagrees. Glang et al. teach a process for fabricating a polycrystalline silicon film resistor, which includes deposition of a polycrystalline

silicon layer of very fine grain size upon an insulator surface, followed by ion implantation of boron equal or slightly in excess of the solubility limit of the polycrystalline silicon. The process further includes one or two annealing steps to control the grain size of the polycrystalline silicon layer, to homogenize the dopant distribution and to raise the dopant concentration.

Furthermore, Glang et al. teach a process for fabricating a bipolar transistor as shown Fig. 2 thereof. The base region 40 (P) and the P⁺ extrinsic base 38 are formed in the following manner. A P⁺ boron doped polycrystalline silicon layer 34 is produced and a heat treatment is carried out in order to drive the boron into the monocrystalline silicon below the polycrystalline silicon layer 34, thus creating the P⁺ extrinsic base 38. Thereafter, the polycrystalline silicon layer 34 is removed from the emitter area and a further polycrystalline silicon layer 44 is deposited. The layer 44 is, in a first step, doped with boron and then, after a first anneal step, doped with arsenic. A second annealing step is utilized to fully drive in the boron to form the base region and simultaneously therewith drive in the arsenic to form the emitter region 42 of the transistor.

Accordingly, Glang et al. disclose a process whereby dopant material is always brought into monocrystalline silicon.

There is no process step in which dopant material is removed from the monocrystalline silicon. If there is too high of a P doping (boron) in the designated base region, this is compensated by a corresponding N doping (arsenic) so that the required level of P-doping results.

The disclosed prior art in combination with Glang et al. teach doping a semiconductor blank, e.g., by ion implantation, until a certain concentration is reached. Tempering steps are carried out, in order to anneal the damage occurred during the dopant implantation and to smooth the dopant density throughout the material. However, with the processes of the disclosed prior art and Glang et al., dopant material is always brought into monocrystalline silicon.

The invention of the instant application teaches a different approach: firstly forming an evenly doped area within a semiconductor blank ("window"); secondly covering part of this area in a self-adjusting manner with respect to an edge, so that even small areas which are not accessible by masking with photoresist layers etc. can be covered; and thirdly applying a second tempering step in order to reduce the dopant concentration in the uncovered region. Neither the disclosed prior art nor Glang et al. teach a method of this type.

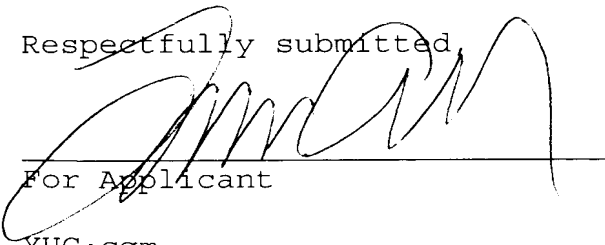
It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since all of the dependent claims are ultimately dependent on claim 1, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1-12 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made. Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,



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